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PTO/SB/33 (07-05)
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# PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): Fang 2-4

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on _____

Signature _____

Typed or printed name _____

| Application Number | Filed |
|---|---|
| 10/776,701 | 2/11/04 |

First Named Inventor: Fang et al.

| Art Unit | Examiner |
|---|---|
| 2627 | Daniell L. Negron |

Applicant requests review of the final rejection in the above-identified application No amendments are being filed with this request

This request is being filed with a notice of appeal

The review is requested for the reason(s) stated on the attached sheet(s)
Note: No more than five (5) pages may be provided

I am the

- [ ] applicant/inventor
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3 73(b) is enclosed (Form PTO/SB/96)
- [X] attorney or agent of record Registration number 36,597
- [ ] attorney or agent acting under 37 CFR 1 34 Registration number if acting under 37 CFR 1 34 _____

Kevin M. Mason
Signature

Kevin M. Mason
Typed or printed name

(203) 255-6560
Telephone number

May 22, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS **SEND TO: Mail Stop AF, Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Patent Application**

Applicant(s): Fang et al.
Case: 2-4
Serial No.: 10/776,701
Filing Date: February 11, 2004
Group: 2627
Examiner: Daniell L. Negron

Title: Impedance-Matched Write Circuit with Shunted Matching Resistor

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MEMORANDUM IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the outstanding final Office Action dated March 16, 2007, Applicants submit the following Pre-Appeal Brief. The present invention and prior art have been summarized in Applicants' prior responses.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The present application was filed on February 11, 2004 with claims 1 through 21. Claims 1-21 are presently pending in the above-identified patent application. Claims 11, 12, and 16-18 are rejected under 35 U.S.C. §102(b) as being anticipated by Leighton et al. (United States Patent Number 6,512,646), and claims 13, 14, and 19 are rejected under 35 U.S.C. §103(a) as

being unpatentable over Leighton et al. The Examiner indicated that claims 1-10 are allowed, and that claims 15, 20, and 21 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

## ARGUMENTS

### Independent Claims 11 and 17

Independent claims 11 and 17 were rejected under 35 U.S.C. §102(b) as being anticipated by Leighton et al. Regarding claim 1, the Examiner asserts that Leighton discloses means for shunting ($Q_7$, $Q_8$) at least a portion of the current that would otherwise pass through the at least one resistor during an overshoot mode (col. 5, lines 7-42).

The present disclosure teaches that

> an ***impedance matched*** *write circuit* is provided that *shunts one or more* ***matching*** *resistors*. The impedance matched write circuit includes an interconnect for connecting to a write head and *at least one resistor between a control voltage and the interconnect* ***for impedance matching to the interconnect***. In one implementation, *a transistor is connected across the resistor to shunt current that would otherwise pass through the resistor during an overshoot mode*. The transistor may be a P-Channel Metal Oxide Silicon (PMOS) transistor or a combination of PMOS and NMOS transistors. A gate voltage of the transistor is controlled by a source such that the transistor is turned on in an overshoot mode and turned off during a steady state mode.
> (Page 2, lines 11-19; emphasis added.)

Applicants note that a "shunt" is defined as "a conductor having low resistance in ***parallel with another device*** to divert a fraction of the current." (See, dictionary.com.) A person of ordinary skill in the art would ***not*** view transistors $Q_7$, $Q_8$ as "shunting" resistors $R_{PA1}$ and/or $R_{PA2}$. For example, Leighton teaches that "transistor Q7 remains on until the delay period is over, and transistor Q8 likewise remains off until the delay period is over." (Col. 5, lines 16-18.) Leighton also teaches that "after the expiration of the delay period, $V_X$ (delay) switches high and $V_Y$ (delay) switches low, such that transistor Q8 turns on and transistor Q7 turns off." (Col. 5, lines 37-39.) Leighton does *not*, however, disclose or suggest that Q7 and Q8 are turned on at the same time. Thus, while current may pass through Q7 or Q8, current does *not* pass through

both Q7 and Q8, and therefore there is ***no*** *shunting of current that would otherwise pass through at least one resistor, wherein the one resistor is a resistor between a control voltage and an interconnect for impedance matching and wherein, by definition, shunting is low resistance conduction in* ***parallel with the resistor,*** as required by the independent claims and the well known definition of a shunt.

Furthermore, the flow of current through each of said transistors to ground would *not* constitute the shunting of current in ***parallel*** *with said resistor*, as required by the independent claims and the well known definition of a shunt, and would *not* constitute ***low*** *resistance conduction* in relation to the current passing through said resistor, as would be apparent to a person of ordinary skill in the art. This analysis applies to the case where only Q7 or Q8 is turned on, and to a case where Q7 and Q8 are turned on at same the time.

Finally, regarding the Examiner's assertion that "the limitations of the rejected claims to not require a transistor to be connected across any resistor nor do they require a transistor to be connected directly to the terminals of any resistor," Applicants note that independent claims 11 and 17 require *means for* ***shunting*** *at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode, wherein said one resistor is a resistor between a control voltage and an interconnect for impedance matching and wherein, by definition, shunting is low resistance conduction in* ***parallel with the resistor***.

Thus, Leighton et al. do not disclose or suggest at least one resistor between a control voltage and said interconnect for impedance matching to said interconnect; and means for shunting at least a portion of the current that would otherwise pass through said at least one resistor during an overshoot mode, as required by independent claims 11 and 17.

Dependent Claims 2-10, 12-16 and 18-21

Dependent claims 12, 16, and 18 were rejected under 35 U.S.C. §102(b) as being anticipated by Leighton et al., and claims 13, 14, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Leighton et al.

Claims 2-10, 12-16, and 18-21 are dependent on claims 1, 11, and 17, respectively, and are therefore patentably distinguished over Leighton et al. because of their

dependency from independents claim 1, 11, and 17 for the reasons set forth above, as well as other elements these claims add in combination to their base claim. The Examiner has already indicated that claims 1-10 are allowed, and that claims 15, 20, and 21 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

All of the pending claims, i e , claims 1-21, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

Kevin M. Mason

Date: May 22, 2007

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